AF 2200

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Roy E. Scheuerlein, et al.		
Title:	MULTIPLE TWIN CELL NON-VOLATILE MEMORY ARRAY AND LOGIC BLOCK STRUCTURE AND METHOD THEREFOR		
Application No.:	10/675,212	Filed:	September 30, 2003
Examiner:	Ho, Hoai V.	Group Art Unit:	2827
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APPEAL BRIEF (37 C.F.R. § 41.37)

This brief is in furtherance of the Notice of Appeal, filed on March 9, 2006. The fee required under 37 C.F.R. § 41.20(b)(2) is provided in the accompanying Transmittal or as set forth in an electronic submission of this paper.

REAL PARTY IN INTEREST

The real party in interest in this appeal is SanDisk 3D LLC, the assignee of record, as evidenced by the assignment recorded at Reel/Frame 015351/0058, and by the merger document recorded at Reel/Frame 017544/0769.

RELATED APPEALS AND INTERFERENCES

Known prior and pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal include:

None.

STATUS OF CLAIMS

Claims 1-8, 10-24, and 26-56 are pending. All claims stand as rejected. Rejected claims 1-8, 10-24, and 26-56 are the subject of this appeal.

STATUS OF AMENDMENTS

An amendment under 37 C.F.R. § 116 (the "Rule 116 Amendment") was submitted with the Notice of Appeal on March 9, 2006 in order to place the application in better form for appeal. In the advisory action mailed April 14, 2006, no indication was provided as to whether the Rule 116 Amendment was or was not entered for purposes of appeal. Applicant believes that the Rule 116 Amendment was proper and has been or will be entered, and the above-mentioned status of claims reflects such entry of the Rule 116 Amendment.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to a non-volatile memory cell array (for example, array 100 shown in Fig. 1) comprising within a first array block a first plurality (107) of X-lines (W5, W6, W7, W8) configured to be individually selected in a write mode of operation (decoders 102 and 106) and configured to be simultaneously selected in a read mode of operation (decoders 102 and 106), and each associated with a first Y-line group (BL1) numbering at least one Y-line (the association arising from a respective memory cell coupled to each respective X-line W5, W6, W7, W8 and to the Y-line BL1. See page 6, lines 2-4, 7-14, 18-22, and page 7, lines 1-2, 12-13.

Another exemplary array 220 depicted in Fig. 6 comprises within a first array block a first plurality (232) of X-lines (W1, W2, W3, W4) configured to be individually selected in a write mode of operation (decoder 222) and configured to be simultaneously selected in a read mode of operation (decoder 222), and each associated with a first Y-line group (234) numbering at least one Y-line (BL1, BL2, BL3, BL4) (the association arising from memory cells 236). See page 11, lines 7-10, 15, and page 10, lines 29-30 for the association of each X-line with the Y-line group.

Claim 29 is directed to a method of operating a non-volatile memory array (for example, memory array 220 depicted in Fig. 6). The method includes programming individual memory

cells associated with a first X-line group (232) of at least one X-line (W1, W2, W3, W4) within a first array block and further associated with a first Y-line group (234) of at least one Y-line (BL1, BL2, BL3, BL4) within the first array block until a desired first aggregate memory cell read current (page 12, lines 9-10) is obtained when simultaneously selecting all the first group of X-lines (decoder 222) and all the first group of Y-lines (decoder 226), at least one of the first X-line group (232) and first Y-line group (234) including more than one such X-line or Y-line. The method also includes reading the memory array by simultaneously selecting all the first group (232) of X-lines and all the first group (234) of Y-lines and generating a signal (signal bus 228; READ DATA) responsive to the first aggregate memory cell read current (page 12, lines 11-14).

Claim 38 is directed to an integrated circuit comprising a memory array (for example, memory array 220 depicted in Fig. 6). The memory array includes a plurality of X-lines (WL1, WL2, ..., WL8) disposed on at least one layer of the memory array. The memory array further includes a plurality of Y-lines (BL1, BL2, ..., BL8) disposed on at least one other layer of the memory array. The memory array further includes a plurality of non-volatile memory cells (the 64 depicted memory cells shown in Fig. 6), each coupled to an associated one of the plurality of X-lines and an associated one of the plurality of Y-lines. The memory array further includes an X-line selection circuit (222) for selecting within a first array block at least a first X-line group (232) of at least two X-lines (WL1, WL2, WL3, WL4) when in a read mode, and for selecting a lesser number of X-lines within at least the first X-line group (232) when in a write mode (decoder 222, selecting one such X-line to "program" or write). The memory array further includes a Y-line selection circuit (226) for simultaneously selecting within the first array block in the read mode a first Y-line group (234) of at least one Y-line (BL1, BL2, BL3, BL4) and a second Y-line group (235) of at least one Y-line (BL5, BL6, BL7, BL8), and for respectively coupling the selected first and second Y-line groups to respective first and second inputs (conveyed by signal buses 228, 229) of an associated sense amplifier circuit (230). The associated sense amplifier circuit is responsive to an aggregate signal (signal bus 228, see page 12, lines 9-14) from memory cells (236) associated with both the selected first X-line group (232) and the selected first Y-line group (234), and responsive to an aggregate signal (signal bus 229) from memory cells (237) associated with both the selected first X-line group (232) and the selected second Y-line group (235). See generally pages 11-12, and more specifically, page 11, lines 7-10, 15-19, and page 12, lines 9-14.

Claim 51 is directed to an integrated circuit comprising a memory array (for example, memory array 220 depicted in Fig. 6). The memory array includes a plurality of X-lines (WL1, WL2, ..., WL8) disposed on at least one layer of the memory array. The memory array further includes a plurality of Y-lines (BL1, BL2, ..., BL8) disposed on at least one other layer of the memory array. The memory array further includes a plurality of non-volatile memory cells (the 64 depicted memory cells shown in Fig. 6), each coupled to an associated one of the plurality of X-lines and an associated one of the plurality of Y-lines. The memory array further includes means for programming individual memory cells associated with a first X-line group (232) of at least one X-line within a first array block and further associated with a first Y-line group (234) of at least one Y-line within the first array block (the integrated circuit, including decoders 222, 226, and including circuitry as stated at page 11, lines 25-29) until a desired aggregate memory cell read current is obtained (page 12, lines 9-10) when simultaneously selecting all the first group (232) of X-lines and all the first group (234) of Y-lines, at least one of the first X-line group (232) and first Y-line group (234) including more than one such X-line or Y-line. The memory array further includes means for reading the memory array by simultaneously selecting all the first group of X-lines (decoder 222) and all the first group of Y-lines (decoder 226) and generating a signal (signal bus 228; signal READ DATA from sense amplifier 230) responsive to the aggregate memory cell read signal conveyed on the first group (234) of Y-lines.

The foregoing concise explanations of the subject matter defined in each of the above-identified claims, and the corresponding references to the specification and to the drawing, are exemplary and should not to be taken as limiting of the invention.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Ground I: The rejection of claim 1 (and thus its dependent claims 2-14 and 26-28) under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention (to the extent that this rejection has not already been overcome by entry and consideration of the Rule 116 Amendment).

Ground II: The rejection of claim 1 (and thus its dependent claims 2-14 and 26-28) under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention (to the extent that this rejection has not already been overcome by entry and consideration of the Rule 116 Amendment).

Ground III: The rejection of claims 1, 2, 8, 9 (now canceled and substantially incorporated into claim 1), 13, 14, 18-24, 26-30, 32-33, 37-38, 40-43, 46, 50-53 and 56 under 35 U.S.C. § 102(a) as being anticipated by La Rosa (U.S. Patent No. 6,738,286).

Ground IV: The rejection of claims 1-5, 8, 13, 14, 18, 27-30, 32-33, 38, 40, 41, 46, 50-53 and 56 under 35 U.S.C. § 102(b) as being anticipated by Zink et al. (U.S. Patent No. 5,946,241).

Ground V: The rejection of claims 10-12, 14-17, 26, 31, 34-36, 44, 45, 47-49, 54, and 55 under 35 U.S.C. § 103(a) as being unpatentable over La Rosa (U.S. Patent No. 6,738,286) or Zink et al. (U.S. Patent No. 5,946,241).

ARGUMENT

Ground I: The rejection of claims 1-14 and 26-28 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention (to the extent that this rejection has not already been overcome by entry of the Rule 116 Amendment).

Claims 1-14 and 26-28

Claim 1 presently recites (consistent with entry of the Rule 166 Amendment):

> 1. A non-volatile memory cell array comprising within a first array block a first plurality of X-lines configured to be individually selected in a write mode of operation and configured to be simultaneously selected in a read mode of operation, and each associated with a first Y-line group numbering at least one Y-line.

This language clarifies that the (previously-recited as "independently selectable") X-lines may be individually selected in a write (i.e., programming) mode of operation. This limitation is not at all inconsistent with those same X-lines being simultaneously selected in a read mode of operation.

This limitation is well supported in the specification as originally filed, including the passage which states:

> During *programming*, *one* of these four word lines 232 is selected at any one time (responsive to decode signals not shown), whereas during *read* mode *all four* word lines 232 are *simultaneously selected* (assuming, of course, that the input signal WLIN1 is selected). Similarly, word line decoder 224 generates a group 233 of four word lines WL5, WL6, WL7, WL8. For the present description, assume that only one input signal WLIN1, WLIN2, is active at any time, and that consequently, only one word line *group of four word lines* is selected during read mode of operation, and *only one word line* itself is selected during programming mode.

(page 11, paragraph 1041, emphasis added). The limitations presently recited in claim 1 include substantially those recited in claim 9 (now canceled). As originally filed, claim 9 recited "wherein each of the first plurality of X-lines is logically independent in a write-mode of operation," and thus provides additional support that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 2-14 and 26-28 stand rejected solely for their dependence from claim 1, and are not argued separately.

Appellant respectfully submits that the limitations recited in claim 1 are well supported in the originally-filed specification, and urges this honorable Board to reverse this rejection.

Ground II: The rejection of claims 1-14 and 26-28 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention (to the extent that this rejection has not already been overcome by entry of the Rule 116 Amendment).

Claims 1-14 and 26-28

Claim 1 presently recites:

> 1. A non-volatile memory cell array comprising within a first array block a first plurality of X-lines configured to be individually selected in a write mode of operation and configured to be simultaneously selected in a read mode of operation, and each associated with a first Y-line group numbering at least one Y-line.

This language clarifies that the (previously-recited as "independently selectable") X-lines may be individually selected in a write (i.e., programming) mode of operation. This limitation is not at all inconsistent with those same X-lines being simultaneously selected in a read mode of operation.

Appellant respectfully submits that any alleged confusion between "independently selectable" and "simultaneously selected during a read mode" in the previously recited phrase "independently selectable X-lines configured to be simultaneously selected in a read mode of operation," as was alleged in the Final Action mailed December 8, 2005, no longer can be sustained from a present reading of claim 1.

Claims 2-14 and 26-28 stand rejected solely for their dependence from claim 1, and are not argued separately.

Appellant urges this honorable Board to reverse this rejection.

Ground III: The rejection of claims 1, 2, 8, 9 (now canceled and substantially incorporated into claim 1), 13, 14, 18-24, 26-30, 32-33, 37-38, 40-43, 46, 50-53 and 56 under 35 U.S.C. § 102(a) as being anticipated by La Rosa (U.S. Patent No. 6,738,286).

Claims 1, 2, 8, 13, 14, 19-21, 24, 27, 28

Regarding claim 1, the Office advances the position that La Rosa discloses in Fig. 3, Fig. 4, and Fig. 6 "a non-volatile memory cell array comprising within a first array block (COL0) a first plurality of 'independently selectable' (Tables 2-5 from column 6 for erasing and writing only) X-lines (WL_m and WL_{m+1}) configured to be simultaneously selected in a read mode of

operation, and each associated with a first Y-line group (BL0 to BL4) numbering at least one Y-line." Specifically, reference is made by the Office to column 6, Tables 2-5, for allegedly disclosing independently selectable X-lines for erasing and writing, and further reference is made to column 6, lines 9-19 as disclosing X-lines configured to be simultaneously selected in a read mode of operation.

The relevant aspect of Fig. 3 described by La Rosa concerns the two zones B1 and B2, which can be read simultaneously and are erasable independently from one another. The word line decoder WLDEC2 is arranged to select the word lines WL_m and WL_{m+1} simultaneously during a reading operation (see column 5, lines 25-31). Such a description does not include any insight as to the details of zones B1 and B2, and thus Fig. 3 taken alone provides no teaching or suggestion of relevance to any of the claims.

La Rosa provides an example of such zones B1 and B2 in Fig. 4, which shows a word line WL_m associated with zone B1 and another word line WL_{m+1} associated with zone B2. These two word lines WL_m and WL_{m+1} are described as being simultaneously selected in a read mode, but each of the two word lines is associated with its own group of bit lines. Specifically, word line WL_m is only associated with bit-lines BL5-BL7 and is *not* associated with bit lines BL0-BL4, whereas the other word line WL_{m+1} is only associated with bit-lines BL0-BL4 and is *not* associated with bit lines BL5-BL7. For example, La Rosa recites:

> *According to the invention*, the drains D of the access transistors AT of the cells C10, C11, C12, C13 and C14 of the zone B1 are not connected to the bit lines BL_0, BL_1, BL_2, BL_3, BL_4 and the drains D of the access transistors AT of the cells C25, C26, C27 of the zone B1 are not connected to the bit lines BL_5, BL_6, BL_7. The absence of the connections are illustrated in the figure by circled crosses.

(column 6, lines 1-7, emphasis added) La Rosa is not describing the mere programming state of the memory cells in zones B1 and B2, but rather is describing whether each memory cell is even connected to any bit line at all.

A word line cannot be considered as being associated with a bit line unless a memory cell is coupled between such a word line and such a bit line. (See the instant application's consistent usage of "associated", such as on page 2 at lines 7-9, on page 10 at lines 29-30, and elsewhere.)

La Rosa includes the "non-useful" memory cells (e.g., C10-C14) to simplify the mask implications of zones B1 and B2, and to ensure that other cells which are coupled to both a word line and a bit line are consistent with the memory cells elsewhere in the array (see column 7 at lines 55-59, and column 8 at lines 6-9). Such non-useful memory cells are *not associated* with the bit line to which it could have been connected, but in fact is not connected. Said differently, even though a word line traverses across a bit line (whether above or below the semiconductor layer in which the bit lines are formed), such a word line is not associated with bit line unless there is a memory cell coupled to both such lines.

As another example, La Rosa drives home this structural distinction with the following:

> It follows from the foregoing that *an essential and sufficient characteristic* for simultaneous reading of the special bits of the first and of the second type is that a line of bits connected to a useful memory cell of a special zone is not connected to a useful memory cell of the other special zone.

(column 7, lines 60-64, emphasis added) With this teaching strongly set forth by La Rosa, it is clear that the word lines WL_m and WL_{m+1} are not *both* associated with the bit lines BL0-BL4, nor are they *both* associated with the bit lines BL5-BL7. The position advanced by the Office disagrees squarely with this statement, but Appellant respectfully submits the Office is mistaken. Each respective word line is associated with a respective group of bit lines that are *not* also associated with the other word line. Thus even though Fig. 4 shows a non-volatile memory cell array comprising within a first array block a first plurality of X-lines configured to be simultaneously selected in a read mode of operation, Fig. 4 does *not* show that each of such first plurality of X-lines is associated with a first Y-line group numbering at least one Y-line. Thus, Fig. 4 does not teach or suggest all the limitations of the claim.

In Fig. 6 La Rosa describes another embodiment of such zones B1 and B2 shown in Fig. 3. The distinctions as between WL_m and WL_{m+1} set forth above are also true in this figure, since the word line WL_m is only associated with the bit line group including BL5-BL7, whereas the word line WL_{m+1} is only associated with the bit line group including BL0-BL4.

Fig. 6 also depicts zones B1' and B2' in addition to zones B1 and B2. The word line WL_m' of the zone B1' is connected to the word line WL_m of the zone B1, and the word line

WL_{m+1}' of the zone B2' is connected to the word line WL_{m+1} of the zone B2. (The La Rosa specification at column 8, lines 10-13 is clearly in error (e.g., referring to WL_{m+1} being in zone B1 and WL_{m+1}' being in zone B1' when compared to the figure itself.) La Rosa continues with:

> The valid cells of the zones B1' and B2' are in this case *read*, *erased*, then *programmed* at the same time as the corresponding memory cells of the zones B1 and B2. The condition and configuration bits are then subject to a double storing (redundancy), which represents an insurance factor in case of a failing useful memory cell of the zone B1 or of a useful memory cell of the zone B2.

(column 8, lines 13-19, emphasis added) To accomplish this functionality (and as Fig. 6 shows) the word lines WL_m and WL_m' are connected together, and so are simultaneously selected during a read mode, during an erase mode, and during a program mode of operation. Likewise, the word lines WL_{m+1} and WL_{m+1}' are connected together, and so are simultaneously selected during a read mode, during an erase mode, and during a program mode of operation. La Rosa provides no teaching for any mode of operation not consistent with such a pair of word lines being connected together (and thus either both selected or both unselected for *all* operation modes).

Regarding claim 2, Appellant notes that the Office advances the position that La Rosa discloses in Fig. 3 that each of the first plurality of X-lines is also associated with a second Y-line group, which is identified as BL5 to BL7. As described above, Fig. 3 is useful for identifying the *zones* B1 and B2 which La Rosa decribes, but not for ascertaining which word lines are associated with which bit lines. As further described above, the word line WL_m is associated with bit lines BL5 to BL7, and the word line WL_{m+1} is associated with bit lines BL0 to BL4.

Appellant respectfully submits that a prima facie rejection has not been made out as to claim 1, as the cited reference does not teach all the limitations of the claim.

Claims 18, 22

The Office has not identified any portion of La Rosa that allegedly teaches or suggests the limitations of these claims. Appellant submits that no prima facie case of anticipation has been made, as La Rosa does not teach or suggest any capability for performing threshold logic upon one or more inputs to the array, as recited in the claim.

Claim 23

The Office has not identified any portion of La Rosa that allegedly teaches or suggests the limitations of this claim. Appellant submits that no prima facie case of anticipation has been made, as La Rosa does not teach or suggest any capability for performing weighted input threshold logic upon one or more inputs to the array, as recited in the claim.

Claim 26

The Office has not identified any portion of La Rosa that allegedly teaches or suggests the limitations of this claim. Appellant submits that no prima facie case of anticipation has been made, as La Rosa does not teach or suggest any configuration of a content addressable memory array, as recited in the claim.

Claims 29, 32, 33, 37, 51-53, and 56

The Office has not identified any portion of La Rosa that allegedly teaches or suggests the limitations of these claims. As an exemplary claim, independent claim 29 in relevant part recites:

> programming *individual* memory cells associated with a first X-line group of at least one X-line within a first array block and further associated with a first Y-line group of at least one Y-line within the first array block until a desired first *aggregate* memory cell read current is obtained *when simultaneously selecting* all the first group of X-lines and all the first group of Y-lines, at least one of the first X-line group and first Y-line group including more than one such X-line or Y-line; and
>
> reading the memory array by *simultaneously* selecting all the first group of X-lines and all the first group of Y-lines and generating a signal responsive to the first *aggregate* memory cell read current.

Appellant refers to the description above for the general description of La Rosa's memory array. There is no teaching or suggestion in La Rosa for programming individual memory cells associated with a first X-line group ... and further associated with a first Y-line group ... until a desired *aggregate* current is obtained when *when simultaneously selecting* all the first group of X-lines and all the first group of Y-lines. Fig. 6 shows memory cells that are read, erased, and programmed simultaneously, but no teaching is found for programming until an aggregate current is reached.

As the Office has not identified any portion of La Rosa that allegedly teaches or suggests such limitations, Appellant respectfully submits that the Office has not made out a prima facie case for anticipation of these claims. Moreover, Appellant respectfully submits that La Rosa provides no basis for anticipation, whether identified or not.

Claim 30

The Office has not identified any portion of La Rosa that allegedly teaches or suggests the limitations of this claim. Claim 30 in relevant part recites:

> programming individual memory cells associated with the first X-line group and further associated with a *second* Y-line group of at least one Y-line until a desired *second* aggregate memory cell read current is obtained when simultaneously selecting all the first group of X-lines and all the second group of Y-lines, *which second aggregate memory cell current is greater than the first aggregate memory cell current*; and
>
> reading the memory array by *simultaneously selecting* all the first group of X-lines and all the *first and second* groups of Y-lines and generating a signal responsive to the *greater* of the first and second aggregate memory cell read current.

Appellant refers to the description above for the general description of La Rosa's memory array. There is no teaching or suggestion in La Rosa for programming individual memory cells associated with a first X-line group ... and further associated with a second Y-line group ... until a desired *second aggregate* current is obtained when *simultaneously selecting* all the first group of X-lines and all the second group of Y-lines, *which second aggregate memory cell current is greater than the first aggregate memory cell current*. Moreover, there is no teaching or suggestion in La Rosa for reading the memory array by *simultaneously selecting* all the first group of X-lines and all the *first and second* groups of Y-lines and generating a signal responsive to the *greater* of the first and second aggregate memory cell read current.

Fig. 6 shows memory cells that are read, erased, and programmed simultaneously, but no teaching is found for programming until an aggregate current is reached. Nor does the structure of Fig. 6 disclose other requisite limitations of the claim, as described above.

As the Office has not identified any portion of La Rosa that allegedly teaches or suggests such limitations, Appellant respectfully submits that the Office has not made out a prima facie

case for anticipation of these claims. Moreover, Appellant respectfully submits that La Rosa provides no basis for anticipation, whether identified or not.

Claims 38, 40-43, 46, and 50

The Office has not identified any portion of La Rosa that allegedly teaches or suggests the limitations of these claims. Independent claim 38 in relevant part recites:

> ... a Y-line selection circuit for simultaneously selecting within the first array block in the read mode a first Y-line group of at least one Y-line and a second Y-line group of at least one Y-line, and for respectively coupling the selected first and second Y-line groups to respective first and second inputs of an associated sense amplifier circuit;
> wherein the associated sense amplifier circuit is responsive to an *aggregate* signal from memory cells associated with *both* the selected *first X-line group* and the selected *first Y-line group*, and responsive to an *aggregate* signal from memory cells associated with *both* the selected *first X-line group* and the selected *second Y-line group*.

Appellant refers to the description above for the general description of La Rosa's memory array. There is no teaching or suggestion in La Rosa describing the above limitations. La Rosa shows in Fig. 3 a group of sense amplifier circuits, each coupled to a single selected bit line (see column 5, lines 1-8 and lines 33-40, and especially column 6, lines 9-12). Nowhere is a sense amplifier disclosed that is responsive to any kind of a signal from two different bit lines, let alone the additional limitations recited in the claim.

As the Office has not identified any portion of La Rosa that allegedly teaches or suggests such limitations, Appellant respectfully submits that the Office has not made out a prima facie case for anticipation of these claims. Moreover, Appellant respectfully submits that La Rosa provides no basis for anticipation, whether identified or not.

For the at least the foregoing reasons, this honorable Board is respectfully requested to reverse this rejection of these claims.

Ground IV: The rejection of claims 1-5, 8, 13, 14, 18, 27-30, 32-33, 38, 40, 41, 46, 50-53 and 56 under 35 U.S.C. § 102(b) as being anticipated by Zink et al. (U.S. Patent No. 5,946,241).

Claims 1-5, 8, 13, 14, 27, and 28

Regarding claim 1, the Office advances the position that Zink discloses in Fig. 3 and Fig. 4 a "non-volatile memory cell array comprising within a first array block (COL_0) a first plurality of 'independently selectable' (column 5, lines 15-21 for erasing and writing only) X-lines (LMjs) configured to be simultaneously selected in a read mode of operation, and each associated with a first Y-line group (BL_0 to BL_7) numbering at least one Y-line."

Applicant respectfully submits that Zink clearly teaches otherwise. Zink teaches a memory architecture having two memory cells per stored bit of information. Each of the two memory cells resides in a respective array block (i.e., "half-array"), and the read circuit (i.e., "sense amplifier" circuit) is preferably disposed between the two array blocks. Zink teaches:

> Preferably, the memory array has two parts that are symmetrical with respect to each of said read circuits owing to the fact that the memory cells of one of these parts are connectable exclusively to one of said first and second terminals of said read circuits while the memory cells of the other part are connectable exclusively to the other of said first and second terminals of said read circuits.
>
> Thus, for each bit, the programmed cell will belong to one part of the memory array while the erased cell will belong to the part that is symmetrical to it.

(column 4, lines 1-10) Zink clearly sets forth two array blocks, separated by a group of read circuits. The selected word line LMj in the upper portion of Fig. 3, and the selected word line LMj in the lower portion of Fig. 3, are thus respectively disposed within *different* array blocks. Zink continues:

> According to the invention, the memory array has programmed and an erased memory cell *on either side of a plurality of read circuits* $CL'_0, \ldots, CL'_7$. Consequently during the reading stage, for each bit of a word only the erased cell consumes current. A read circuit is described here below in FIG. 4.
>
> In order to obtain a perfectly symmetrical memory array, the memory array is *divided into two identical half-arrays*: an upper half-array and a lower half-array. Each half-array is identical to the part of the memory array pertaining to cell C_i described in FIG. 1. Each read circuit $CL'_0, \ldots, CL'_7$ is associated firstly with a plurality of bit lines LB'_0, LB'_i, LB'_{i+7}, ...

> belonging to the upper half-array and secondly to a plurality of bit lines LB'_0, LB'_i, LB'_{i+7}, ... belonging to the lower half-array. Memory cells C_i and C'_i are respectively connected to bit lines LB_i and LB'_i. The read circuits are preferably located between the two half-arrays. The perfect symmetry of the memory array provides for a simultaneous selection of the memory cells C_i and C'_i in both half-arrays.

(column 4, line 51 through column 6, line 3) Zink discloses a memory structure in which more than one word line may be simultaneously activated, but such word lines are located within different half-arrays (i.e., "memory blocks"). In addition, the bit lines within one half-array are distinct from the bit lines within the other half array. Alternatively, if such two word lines are connected together to form a single electrical node, and if such a compound word line is thought of as a single word line, then there is only *one* word line selected at a time.

In Fig. 4, Zink describes a read circuit useful for his invention. In this figure he shows a single word line LMj coupling a memory cell C_i to the bit line LB_i and also coupling a memory cell C'_i to the bit line LB'_i . Since this figure is introduced to describe the read circuit, the word line structure might be assumed to be a non-physical representation of the equivalent circuit shown in Fig. 3 with regard to a selected word line in each of the two half-arrays. However, if this figure is taken to teach a different physical structure than taught by Fig. 3, then the two memory cells C_i and C'_i *could* possibly be thought of as being disposed within a single array block. But if that is the case, then there is only a *single* word line LMj selected at one time during a read operation. It is unlikely that Zink means to suggest this possibility, as the text clearly describes Fig. 4 in the context of Fig. 3:

> FIG. 4 shows a read circuit CL'_k of the non-volatile memory according to the invention. This read circuit is connected firstly to bit line LB_i and secondly to bit line LB'_i. *According to FIG. 3*, memory cells C_i and C'_i are connected respectively to bit lines LB_i and LB'_i and are selected by word line LM_j. Upon receipt of signal COL_p, the p_{th} word is read, by coupling eight respective bit lines LB_i through LB_{1+7} [sic] and LB'_i through LB'_{1+7} [sic] to their respective reading circuits CL'_0 through CL'_7.
> *[NOTE: the subscripts "1+7" clearly should be "i+7"]*

(column 5, lines 41-49) However, under either assumption, it is still clear that Zink does not teach or suggest a non-volatile memory cell array comprising *within a first array block* a first plurality of X-lines configured to be *individually selected* in a write mode of operation and

configured to be *simultaneously selected in a read mode of operation*, and each associated with a first Y-line group numbering at least one Y-line.

Claim 18

The Office has not identified any portion of Zink that allegedly teaches or suggests the limitations of this claim. Appellant submits that no prima facie case of anticipation has been made, as Zink does not teach or suggest any capability for performing threshold logic upon one or more inputs to the array, as recited in the claim.

Claims 29, 32, 33, 51-53, and 56

The Office has not identified any portion of Zink that allegedly teaches or suggests the limitations of these claims. As an exemplary claim, independent claim 29 in relevant part recites:

> programming *individual* memory cells associated with a first X-line group of at least one X-line within a first array block and further associated with a first Y-line group of at least one Y-line within the first array block until a desired first *aggregate* memory cell read current is obtained *when simultaneously selecting* all the first group of X-lines and all the first group of Y-lines, at least one of the first X-line group and first Y-line group including more than one such X-line or Y-line; and
> reading the memory array by *simultaneously* selecting all the first group of X-lines and all the first group of Y-lines and generating a signal responsive to the first *aggregate* memory cell read current.

Appellant refers to the description above for the general description of Zink's memory array. There is no teaching or suggestion in Zink for programming individual memory cells associated with a first X-line group ... and further associated with a first Y-line group ... until a desired *aggregate* current is obtained when *when simultaneously selecting* all the first group of X-lines and all the first group of Y-lines. Fig. 6 shows memory cells that are read, erased, and programmed simultaneously, but no teaching is found for programming until an aggregate current is reached.

As the Office has not identified any portion of Zink that allegedly teaches or suggests such limitations, Appellant respectfully submits that the Office has not made out a prima facie

case for anticipation of these claims. Moreover, Appellant respectfully submits that Zink provides no basis for anticipation, whether identified or not.

Claim 30

The Office has not identified any portion of Zink that allegedly teaches or suggests the limitations of this claim. Claim 30 in relevant part recites:

> programming individual memory cells associated with the first X-line group and further associated with a *second* Y-line group of at least one Y-line until a desired *second* aggregate memory cell read current is obtained when simultaneously selecting all the first group of X-lines and all the second group of Y-lines, *which second aggregate memory cell current is greater than the first aggregate memory cell current*; and
>
> reading the memory array by *simultaneously selecting* all the first group of X-lines and all the *first and second* groups of Y-lines and generating a signal responsive to the *greater* of the first and second aggregate memory cell read current.

Appellant refers to the description above for the general description of Zink's memory array. There is no teaching or suggestion in Zink for programming individual memory cells associated with a first X-line group ... and further associated with a second Y-line group ... until a desired *second aggregate* current is obtained when *simultaneously selecting* all the first group of X-lines and all the second group of Y-lines, *which second aggregate memory cell current is greater than the first aggregate memory cell current.* Moreover, there is no teaching or suggestion in Zink for reading the memory array by *simultaneously selecting* all the first group of X-lines and all the *first and second* groups of Y-lines and generating a signal responsive to the *greater* of the first and second aggregate memory cell read current.

As the Office has not identified any portion of Zink that allegedly teaches or suggests such limitations, Appellant respectfully submits that the Office has not made out a prima facie case for anticipation of these claims. Moreover, Appellant respectfully submits that Zink provides no basis for anticipation, whether identified or not.

Claims 38, 40, 41, 46, and 50

The Office has not identified any portion of Zink that allegedly teaches or suggests the limitations of these claims. Independent claim 38 in relevant part recites:

> ... a Y-line selection circuit for simultaneously selecting within the first array block in the read mode a first Y-line group of at least one Y-line and a second Y-line group of at least one Y-line, and for respectively coupling the selected first and second Y-line groups to respective first and second inputs of an associated sense amplifier circuit;
> wherein the associated sense amplifier circuit is responsive to an *aggregate* signal from memory cells associated with *both* the selected *first X-line group* and the selected *first Y-line group*, and responsive to an *aggregate* signal from memory cells associated with *both* the selected *first X-line group* and the selected *second Y-line group*.

Appellant refers to the description above for the general description of Zink's memory array. There is no teaching or suggestion in Zink describing the above limitations. Zink shows in Fig. 3 a group of sense amplifier circuits, each coupled to a single selected bit line (see column 5, lines 1-8 and lines 33-40, and especially column 6, lines 9-12). Nowhere is a sense amplifier disclosed that is responsive to any kind of a signal from two different bit lines, let alone the additional limitations recited in the claim.

As the Office has not identified any portion of Zink that allegedly teaches or suggests such limitations, Appellant respectfully submits that the Office has not made out a prima facie case for anticipation of these claims. Moreover, Appellant respectfully submits that Zink provides no basis for anticipation, whether identified or not.

For the at least the foregoing reasons, this honorable Board is respectfully requested to reverse this rejection of these claims.

Ground V: The rejection of claims 10-12, 14-17, 26, 31, 34-36, 44, 45, 47-49, 54, and 55 under 35 U.S.C. § 103(a) as being unpatentable over La Rosa (U.S. Patent No. 6,738,286) or Zink et al. (U.S. Patent No. 5,946,241).

As argued above in regards to the other grounds of rejection, Appellant respectfully submits that the limitations of the claims from which these identified claims depend are not taught or suggested by La Rosa or Zink. This assertion alone is believed to render this rejection as unsupported. Nonetheless, certain of these claims are argued separately herebelow.

Claims 11, 35, 45, and 55

Regarding claims 11, 35, 45, and 55, the Office advances the position that "[i]t would have been obvious to one having ordinary skill in the art at the time the invention was made to modify La Rosa and Zink' non-volatile EEPROM with the different types of non-volatile memories as the claimed invention since they have the same purpose and advantages to retain recorded information even when the power to the memory is turned off and *since it has been held that constructing a formerly memory structure [sic] in various elements involves only routine skill in the art* (see Zink col. 6, lines 24-32)."

The cited portion of Zink recites:

> Having thus described at least one illustrative embodiment of the invention, various alterations, modifications, and improvements will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended as limiting. The invention is limited only as defined in the following claims and the equivalents thereto.

(column 6, lines 24-32) Each of these claims 11, 35, 45, and 55 recites the additional limitation that the memory array comprises anti-fuse memory cells. As the Office has set forth, Zink describes a non-volatile EEPROM memory array, within which the memory cells can be programmed, read, and erased.

Appellant respectfully submits that a memory array having anti-fuse memory cells, which are likely two-terminal memory cells, and which memory cells likely (although not necessarily) can be programmed only once, is not necessarily suggested by a reference which describes structures and circuits useful for a memory array having EEPROM memory cells which are programmable and erasable three-terminal memory cells.

Appellant respectfully submits that the Office has not made out a prima facie case for anticipation of these claims.

Claims 16 and 48

Claim 16 recites the additional limitation that the memory array comprises a three-dimensional memory array having more than one plane of memory cells (i.e., claim 15 from which it depends) and further recites the additional limitation wherein the first plurality of X-lines comprises X-lines disposed on more than one layer of the memory array. Claim 48 recites the same limitations, and further includes the limitation that said more than one plane of memory cells [are] disposed above a semiconductor substrate (i.e., claim 47 from which it depends).

The Office advances the position that "[i]t would have been obvious to one having ordinary skill in the art at the time the invention was made to modify La Rosa and Zink' memory array with the different dimensional memory array [sic] and disposal [sic] one or more layers of the memory array as the claimed invention, *since it has been held that constructing a formerly [sic] memory array in various dimensions and layers involves only routine skill in the art* (see Zink col. 6, lines 24-32)."

Such a structural limitation is in no way suggested by the off-hand generalizing comment in Zink that is cited by the Office.

Again , this cited portion can hardly be viewed as providing the suggestion alleged by the Office, that would arrive at such a specific structural limitation. Appellant emphatically submits that there is no suggestion in the cited art, nor in general knowledge of one having ordinary skill in the art, for the first plurality of X-lines (or the first group of X-lines), which are simultaneously selected during a read operation, comprising X-lines disposed on more than one layer of the memory array, as recited in these claims (of course, along with the other recited limitations).

CONCLUSION

For the at least the foregoing reasons, this honorable Board is respectfully requested to reverse the rejections of claims 1-8, 10-24, and 26-56 and to direct the claims of the present application to be issued.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

☑ deposited with the US Postal Service with sufficient postage as first class mail and addressed as shown above.

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Date

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Respectfully submitted,

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CLAIMS APPENDIX

1. (Previously presented) A non-volatile memory cell array comprising within a first array block a first plurality of X-lines configured to be individually selected in a write mode of operation and configured to be simultaneously selected in a read mode of operation, and each associated with a first Y-line group numbering at least one Y-line.

2. (Original) The memory array as recited in claim 1 wherein each of the first plurality of X-lines is also associated with a second Y-line group numbering at least one Y-line.

3. (Previously Presented) The memory array as recited in claim 2 wherein the first and second Y-line groups are simultaneously selectable in a read mode and, when so selected, are respectively coupled to true and complement inputs of a sense amplifier circuit.

4. (Original) The memory array as recited in claim 3 wherein the first and second Y-line groups each numbers only one Y-line.

5. (Original) The memory array as recited in claim 3 wherein the first and second Y-line groups each numbers more than one Y-line.

6. (Original) The memory array as recited in claim 3 further comprising a reference signal operably coupled to either the true or complement input of the sense amplifier, wherein the first and second Y-line groups each numbers more than one Y-line.

7. (Original) The memory array as recited in claim 6 wherein the reference signal comprises a reference current.

8. (Previously Presented) The memory array as recited in claim 1 wherein:
the first Y-line group includes more than one Y-line; and
each of the first Y-line group is configured to be simultaneously selected in a read mode of operation.

9. (Canceled)

10. (Original) The memory array as recited in claim 1 wherein the memory array comprises passive element memory cells.

11. (Original) The memory array as recited in claim 10 wherein the memory array comprises anti-fuse memory cells.

12. (Original) The memory array as recited in claim 10 wherein the memory array comprises magnetoresistive memory cells.

13. (Original) The memory array as recited in claim 1 wherein the memory array comprises EEPROM memory cells.

14. (Original) The memory array as recited in claim 1 wherein the memory array comprises a two-dimensional memory array having one plane of memory cells.

15. (Original) The memory array as recited in claim 1 wherein the memory array comprises a three-dimensional memory array having more than one plane of memory cells.

16. (Original) The memory array as recited in claim 15 wherein the first plurality of X-lines comprises X-lines disposed on more than one layer of the memory array.

17. (Previously Presented) The memory array as recited in claim 15 wherein the first plurality of X-lines comprises X-lines disposed only on a single layer of the memory array.

18. (Original) The memory array as recited in claim 2 configured to perform threshold logic upon one or more inputs to the array.

19. (Previously Presented) The memory array as recited in claim 1 further comprising a second plurality of X-lines configured to be simultaneously selected in a read mode of operation and each associated with the first Y-line group.

20. (Previously Presented) The memory array as recited in claim 19 further comprising a third plurality of X-lines associated with the first Y-line group, said third plurality of X-lines being configured, in a read mode of operation, to be simultaneously selected at certain times when the first plurality of X-lines is not selected.

21. (Previously Presented) The memory array as recited in claim 20 further comprising:

a fourth plurality of X-lines associated with the first Y-line group, said fourth plurality of X-lines being configured, in a read mode of operation, to be simultaneously selected when the second plurality of X-lines is not selected; and

a second Y-line group numbering at least one Y-line, each of which is associated with the first, second, third, and fourth pluralities of X-lines.

22. (Original) The memory array as recited in claim 19 configured to perform threshold logic upon one or more inputs to the array.

23. (Original) The memory array as recited in claim 19 configured to perform weighted input threshold logic upon one or more inputs to the array.

24. (Original) The memory array as recited in claim 1 wherein X-lines comprise word lines.

25. (Canceled)

26. (Original) The memory array as recited in claim 1 configured as a content addressable memory array.

27. (Previously Presented) The memory array as recited in claim 2 wherein:

each of the first Y-line group is configured to be simultaneously selected in a read mode of operation; and

each of the second Y-line group is configured to be simultaneously selected in a read mode of operation.

28. (Original) The memory array as recited in claim 1 embodied in computer readable descriptive form suitable for use in design, test or fabrication of an integrated circuit.

29. (Previously Presented) A method of operating a non-volatile memory array comprising:

programming individual memory cells associated with a first X-line group of at least one X-line within a first array block and further associated with a first Y-line group of at least one Y-line within the first array block until a desired first aggregate memory cell read current is obtained when simultaneously selecting all the first group of X-lines and all the first group of Y-lines, at least one of the first X-line group and first Y-line group including more than one such X-line or Y-line; and

reading the memory array by simultaneously selecting all the first group of X-lines and all the first group of Y-lines and generating a signal responsive to the first aggregate memory cell read current.

30. (Original) The method of claim 29 further comprising:

programming individual memory cells associated with the first X-line group and further associated with a second Y-line group of at least one Y-line until a desired second aggregate memory cell read current is obtained when simultaneously selecting all the first group of X-lines and all the second group of Y-lines, which second aggregate memory cell current is greater than the first aggregate memory cell current; and

reading the memory array by simultaneously selecting all the first group of X-lines and all the first and second groups of Y-lines and generating a signal responsive to the greater of the first and second aggregate memory cell read current.

31. (Original) The method of claim 30 wherein the memory array comprises write-once memory cells.

32. (Original) The method of claim 29 further comprising:

programming more than one cell associated with an X-line by simultaneously activating at least two Y-lines.

33. (Original) The method of claim 32 wherein said at least two simultaneously activated Y-lines are associated with different Y-line groups.

34. (Original) The method of claim 29 wherein the memory array comprises passive element memory cells.

35. (Original) The method of claim 34 wherein the memory array comprises anti-fuse memory cells.

36. (Original) The method of claim 34 wherein the memory array comprises magnetoresistive memory cells.

37. (Original) The method of claim 29 wherein the memory array comprises EEPROM memory cells.

38. (Previously Presented) An integrated circuit comprising:

a memory array including:

a plurality of X-lines disposed on at least one layer of the memory array;

a plurality of Y-lines disposed on at least one other layer of the memory array;

a plurality of non-volatile memory cells, each coupled to an associated one of the plurality of X-lines and an associated one of the plurality of Y-lines;

an X-line selection circuit for selecting within a first array block at least a first X-line group of at least two X-lines when in a read mode, and for selecting a lesser number of X-lines within at least the first X-line group when in a write mode; and

a Y-line selection circuit for simultaneously selecting within the first array block in the read mode a first Y-line group of at least one Y-line and a second Y-line group of at least one Y-line, and for respectively coupling the selected first and second Y-line groups to respective first and second inputs of an associated sense amplifier circuit;

wherein the associated sense amplifier circuit is responsive to an aggregate signal from memory cells associated with both the selected first X-line group and the selected first Y-line group, and responsive to an aggregate signal from memory cells

associated with both the selected first X-line group and the selected second Y-line group.

39. (Original) The integrated circuit as recited in claim 38 further comprising a reference signal circuit operably coupled to the second input of the associated sense amplifier circuit.

40. (Original) The integrated circuit as recited in claim 38 wherein the first Y-line group and the second Y-line group each number but one Y-line.

41. (Original) The integrated circuit as recited in claim 38 wherein the associated sense amplifier circuit is configured to sense more than two levels of aggregate memory cell signal.

42. (Original) The integrated circuit as recited in claim 38 wherein:

the X-line selection circuit is further configured for selecting, when in the read mode, a second X-line group of at least two X-lines simultaneously with selecting the first X-line group; and

the associated sense amplifier circuit is responsive to an aggregate signal from memory cells associated with the selected first X-line group and the selected first Y-line group and memory cells associated with the selected second X-line group and the selected first Y-line group, and responsive further to an aggregate signal from memory cells associated with the selected first X-line group and the selected second Y-line group and memory cells associated with the selected second X-line group and the selected second Y-line group.

43. (Previously Presented) The integrated circuit as recited in claim 38 wherein:

the X-line selection circuit is further configured for selecting, when in the read mode, a third X-line group of at least two X-lines when the first X-line group is not selected.

44. (Original) The integrated circuit as recited in claim 38 wherein the memory array comprises passive element memory cells.

45. (Original) The integrated circuit as recited in claim 44 wherein the memory array comprises anti-fuse memory cells.

46. (Original) The integrated circuit as recited in claim 38 wherein the memory array comprises EEPROM memory cells.

47. (Original) The integrated circuit as recited in claim 38 wherein the memory array comprises a three-dimensional memory array having more than one plane of memory cells disposed above a semiconductor substrate.

48. (Previously Presented) The integrated circuit as recited in claim 47 wherein the first X-line group comprises X-lines disposed on more than one layer of the memory array.

49. (Previously Presented) The integrated circuit as recited in claim 47 wherein the first X-line group comprises X-lines disposed only on a single layer of the memory array.

50. (Original) The integrated circuit as recited in claim 38 embodied in computer readable descriptive form suitable for use in design, test or fabrication of said integrated circuit.

51. (Previously Presented) An integrated circuit comprising:

a memory array including:

a plurality of X-lines disposed on at least one layer of the memory array;

a plurality of Y-lines disposed on at least one other layer of the memory array;

a plurality of non-volatile memory cells, each coupled to an associated one of the plurality of X-lines and an associated one of the plurality of Y-lines;

means for programming individual memory cells associated with a first X-line group of at least one X-line within a first array block and further associated with a first Y-line group of at least one Y-line within the first array block until a desired aggregate memory cell read current is obtained when simultaneously selecting all the first group of X-lines and all the first group of Y-lines, at least one of the first X-line group and first Y-line group including more than one such X-line or Y-line; and

means for reading the memory array by simultaneously selecting all the first group of X-lines and all the first group of Y-lines and generating a signal responsive to the aggregate memory cell read signal conveyed on the first group of Y-lines.

52. (Original) The integrated circuit of claim 51 further comprising:

means for programming more than one cell associated with an X-line by simultaneously activating at least two Y-lines.

53. (Original) The integrated circuit of claim 52 wherein said at least two simultaneously activated Y-lines are associated with different Y-line groups.

54. (Original) The integrated circuit of claim 51 wherein the memory array comprises passive element memory cells.

55. (Original) The integrated circuit of claim 54 wherein the memory array comprises anti-fuse memory cells.

56. (Original) The integrated circuit of claim 51 wherein the memory array comprises EEPROM memory cells.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. § 1.130, 1.131, or 1.132 or any other evidence entered by the examiner and relied upon by appellant in the appeal.

RELATED APPEALS APPENDIX

There are no decisions rendered by a court or the Board in any proceeding identified above in the Related Appeals and Interferences section.